

101750252



CAC

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REQUEST FOR CERTIFICATE OF  
CORRECTION UNDER 37 C.F.R. 1.322  
Docket No. SUN-DA-136T  
Patent No. 7,101,759

Jeff Lloyd  
Jeff Lloyd, Patent Attorney, Reg. No. 35,589

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Chang Hun Han  
Issued : September 5, 2006  
Patent No. : 7,101,759 5  
For : Methods for Fabricating Nonvolatile Memory Devices

Mail Stop Certificate of Corrections Branch  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE OF CORRECTION  
UNDER 37 CFR 1.322 (OFFICE MISTAKE)

Sir:

A Certificate of Correction (in duplicate) for the above-identified patent has been prepared and is attached hereto.

In the left-hand column below is the column and line number where errors occurred in the patent. In the right-hand column is the page and line number in the application where the correct information appears.

Patent Reads:

Column 3, line 27:

“fanning”

Column 4, line 2:

“tb-st”

Amendment dated April 10, 2006 Reads:

Claim 8:

--forming--

Claim 8:

--first--

**Certificate**

FEB 22 2007

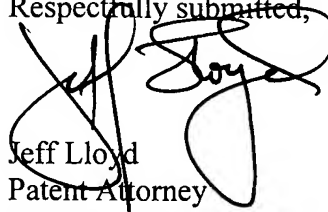
**of Correction**

FEB 22 2007

A true and correct copy of page 3 of the Amendment dated April 10, 2006, which supports Applicants' assertion of the errors on the part of the Patent Office, accompanies this Certificate of Correction.

Approval of the Certificate of Correction is respectfully requested.

Respectfully submitted,



Jeff Lloyd

Patent Attorney

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JL/fes

Attachment: Page 3 of the Amendment dated April 10, 2006.

**COPY**

7. (Previously Presented) A method as defined in claim 1, wherein the polymer layers on the sidewalls of the sacrificial layer are separated by less than a lithographic minimum feature size.

8. (Previously Presented) A method for fabricating a nonvolatile memory device comprising:  
forming an isolation layer and a non-active region in a semiconductor substrate;  
forming an oxide layer and a polysilicon layer on the substrate;  
forming a first sacrificial layer on the polysilicon layer;  
forming a second sacrificial layer on the first sacrificial layer;  
etching the first sacrificial layer using the second sacrificial layer as a mask to form polymer layers on sidewalls of the first and the second sacrificial layers, the polymer layers being generated from the etching of the first sacrificial layer; and  
forming a floating gate and a tunnel oxide using the first and the second sacrificial layers and the polymer layers as an etching mask.

9. (Previously Presented) A method as defined in claim 0, further comprising:  
removing the polymer layers, the first sacrificial layer and the second sacrificial layer; and  
forming an insulating layer and a polysilicon layer over the substrate, the floating gate, and the tunnel oxide.

10. (Previously Presented) A method as defined in claim 0, wherein the polymer layers on the sidewalls of the first and the second sacrificial layers are separated by less than a lithographic minimum feature size.

11. (Previously Presented) A method as defined in claim 0, wherein the second sacrificial layer comprises a patterned photoresistive material.

**FEB 22 2007**

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,101,759

Page 1 of 1

APPLICATION NO.: 10/750,252

DATED : September 5, 2006

INVENTOR : Chang Hun Han

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 3,

Line 27, "fanning" should read --forming--.

Column 4,

Line 2, "tb-st" should read --first--.

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CERTIFICATE OF CORRECTION

PATENT NO. : 7,101,759

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